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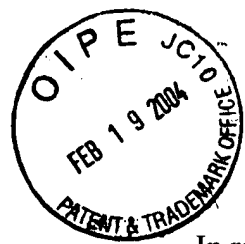
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APPENDIX "A"

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:)	
Lee, et al.)	Confirmation No. 8906
)	
Serial No.: 10/601,959)	Art Unit: 2816
)	
Filed: June 23, 2003)	Examiner: Cunningham, Terry D.
)	
For: A CHARGE PUMP HAVING)	TKHR No. 050324-1321
REDUCED SWITCHING NOISE)	
)	

DECLARATION OF AKBAR ALI

Mail Stop:
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

- 1) I am a named inventor for the above-identified patent application and contributed to the conception of the invention embodied in that patent application.
- 2) I am advised that it has been determined that a reference has been cited against our claimed invention which has a filing date of May 1, 2000.
- 3) Our invention, however, as embodied in the claims of the above-identified patent application, was both conceived and reduced to practice (*i.e.*, made) prior to May of 2000.
- 4) As evidence that the above-identified invention was so conceived and reduced to practice, attached is Exhibit A.

5) Exhibit A is an invention disclosure document used to submit invention disclosures to be reviewed in order to determine whether the invention will be applied for a patent. The entry of this invention disclosure document occurred prior to May 2000 (all dates on the document have been redacted).

I hereby declare that all statements made herein are of my own knowledge are true and that all statements are made on information and belief and are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Feb, 10, 04

Date

Akbar Ali

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REDUCED SWITCHING NOISE)	
)	

DECLARATION OF CHANG-HYEON LEE

Mail Stop:
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P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

- 1) I am a named inventor for the above-identified patent application and contributed to the conception of the invention embodied in that patent application.

- 2) I am advised that it has been determined that a reference has been cited against our claimed invention which has a filing date of May 1, 2000.

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I hereby declare that all statements made herein are of my own knowledge are true and that all statements are made on information and belief and are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

02/09/2004

Date

Lee chun

Chang-Hyeon Lee



C O N E X A N T™

Docket No.: 00CXT0521W
Ranking: NO RANK

1. Title of Innovation

Low Voltage Mode Charge Pump Circuit with Reduced Switching Noise

2. Division/platform Information

Wireless Communications Division

3. Innovator(s)

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Akbar Ali	<p>Personal Information :</p> <p>Home Address : 9802 Eleventh St City : Garden Grove</p> <p>State : CA Zip : 92844</p> <p>Phone : [REDACTED] Fax :</p> <p>Country of Domicile : US Citizenship : US</p> <p>Conexant Contact Information :</p> <p>Address : 4311 Jamboree RoadP. O. Box C, City : Newport Beach</p> <p>State : CA Zip : 92660-3095</p> <p>Phone : [REDACTED] Fax :</p> <p>Email : [REDACTED] Dept. : 776-</p> <p>Mail Code : 601- Supervisor : Mr. Stephen Lloyd</p>

4. Problem Solved

In the design of the clock generator and frequency synthesizer, a charge pump with a PFD generates spurious tones and phase noise by switching noise. This noise is defined as glitch energy and produced by clock feedthrough and charge injection at N or P type of switch. The noise can be reduced by matching of charge currents in both magnitude and time since mismatching generates spurious sidebands in the PLL output. Two types of proposed charge pump circuits are designed with suppression of switching noise for reducing spurious sidebands at the PLL output.

The charge pump cell has two charge pump circuits which are driven by Up and Dw signals. When the PLL is locked, a mismatch of current sources results in the leakage into the loop filter. This effect is periodic and produces sidebands at the output. When Up and Dw switches turn off, charge injection and clock feedthrough results in an error of control voltage, and changes the VCO frequency.

5. Previous Solutions

- 1) The charge pump circuit uses a switch structure that cancels the charge injection by dummy devices. ISSCC96' pp132-133.
- 2) The charge pump circuit uses differential pairs with Down/-down and up/-up, which cancel the charge injection by the opposite signals. ISSCC95' pp112-113

6. Solution

The proposed charge pump shown in Fig. 6.40 suppresses any charge sharing of switching nodes by parasitic capacitance. This is why the switching does not happen at the control voltage node but stays away from it. Moreover, the cascoded stage helps in reducing switching noise by AC coupling to the bias.

This charge pump has common mode feedback to increase the dynamic range of both control voltages. The output voltage of the LPF is almost equal to VCM after locking in the PLL, because the center frequency of the VCO equals the expected clock output of the PLL. The loop filter is fully differential and consists of two second order filters. The small capacitor in the LPF provides for smoothing out the voltage developed across the filter resistors R1 and R2 whenever the charge pump is turned on and off.

If the charge pump is placed under the regulated voltage ($V_c=1.8V$) for a higher PSNR from supply noise, it should be applicable in low voltage operation. A charge pump(II) is proposed in Fig. 6.41 which is more useful in low operating power supply voltage applications.

The charge pump is simplified to two differential input stages, which can prevent switching coupling to the loop filter by having constant voltage sources at the input stages. The differential loop filters are replaced by a loop filter and a constant voltage for saving silicon area, which looks as if operating differentially.

In addition to the proposed charge pump, since the charge pump is operated as 2.2V, the voltage to current converter in the next block should be maximized its common mode voltage range. If the charge pump is used with the proposed V2I converter, it will be beneficial to the low voltage mode charge pump.

I include two attached files for these, one is for the charge pump, the other is the voltage to current converter.



7. Differences/Advantages Over Previous Solutions

In the previous solutions, there are still switching and ac coupled noise shown in Fig 6.43.

In proposed type of charge pumps, the digital switching path is avoided and the digitally coupled noises will be reduced by constance bias.(the simulation result is in Fig 6.44)

8. Status of Innovation

In design If "Other", please specify

9. Product or program in which innovation will be used:

Products Used : Other	Technology Used : Bluetooth
If other, please specify :	If other, please specify :

Additional Information :	
---------------------------------	--

10. Has anyone disclosed or does anyone plan to disclose your innovation outside the Company?

☐ Yes ☒ No ☐ Don't Know

11. Has anyone proposed or does anyone plan to propose a product or program to a customer which includes your innovation?

☐ Yes ☐ No ☒ Don't Know

12. Innovator signature(s): (Do not use black ink)

(CHANG-HYEON LEE) Date : _____

(AKBAR ALI) Date : _____

Qtr Evaluated:

[REDACTED]

Group:

Wireless Communications Division

Technology:

Sub Technology 1:

Sub Technology 2:

Products:

Innovation Block:

Entered:

[REDACTED]

Modified:

[REDACTED]

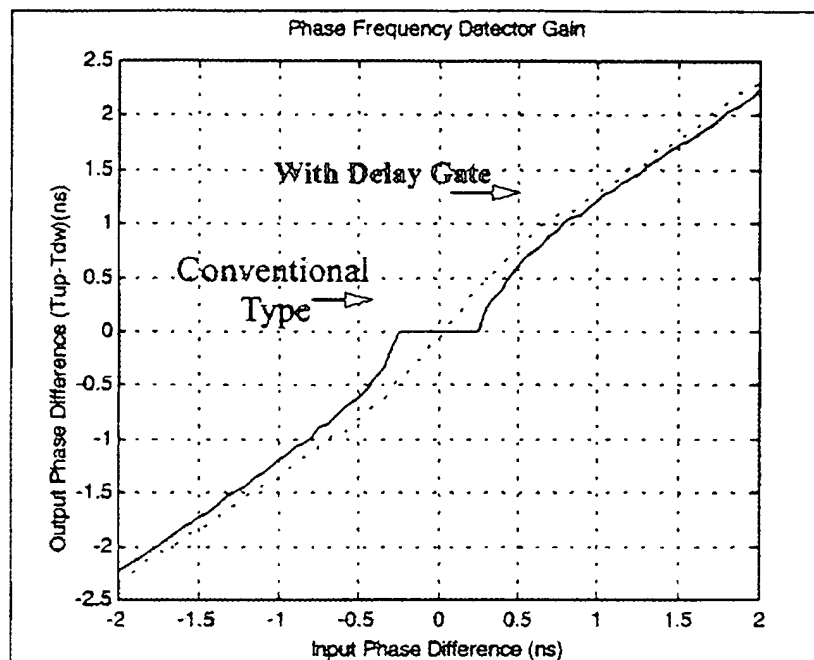


Figure 6.39 D flip-flop PFD transfer function

6.3.6 Charge pump and loop filter (DCP)

In the design of the clock generator and frequency synthesizer, a charge pump with a PFD generates spurious tones and phase noise by switching noise. This noise is defined as glitch energy and produced by clock feedthrough and charge injection at N or P type of switch. The noise can be reduced by matching of charge currents in both magnitude and time since mismatching generates spurious sidebands in the PLL output. Two types of proposed charge pump circuits are designed with suppression of switching noise for reducing spurious sidebands at the PLL output.

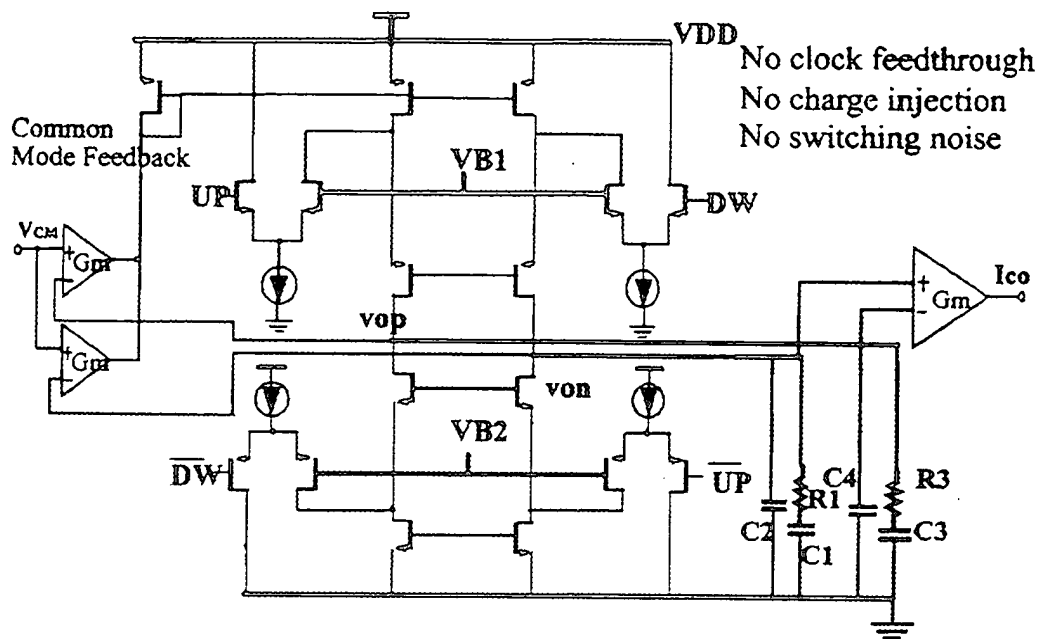


Figure 6.40 The proposed charge pump (I) and differential loop filter

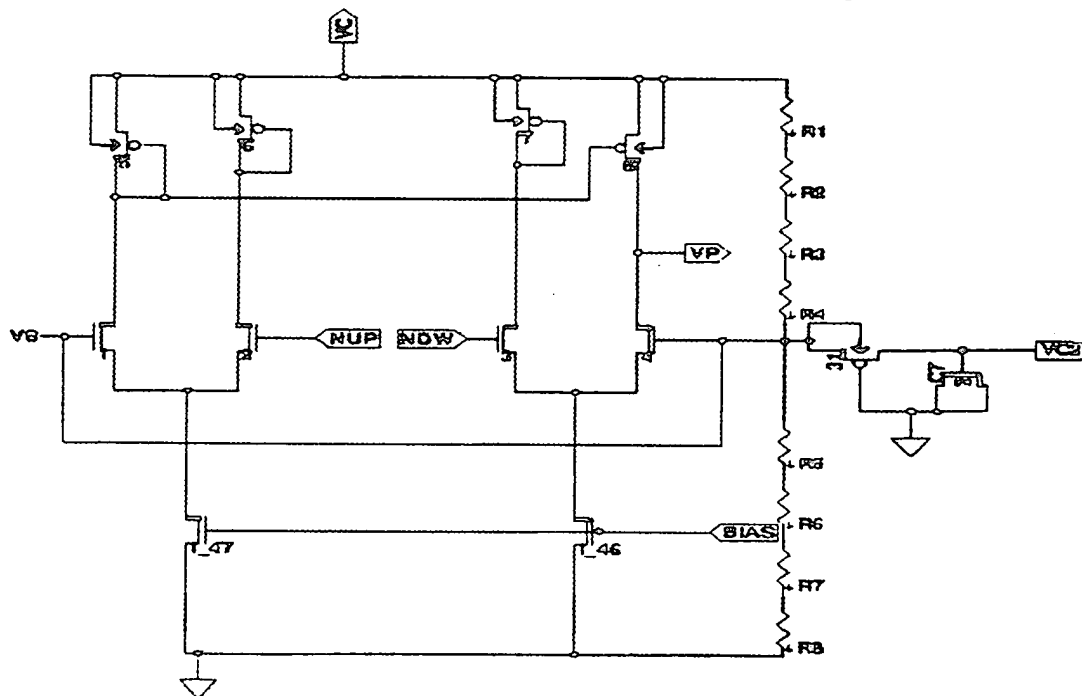


Figure 6.41 The proposed charge pump (II)

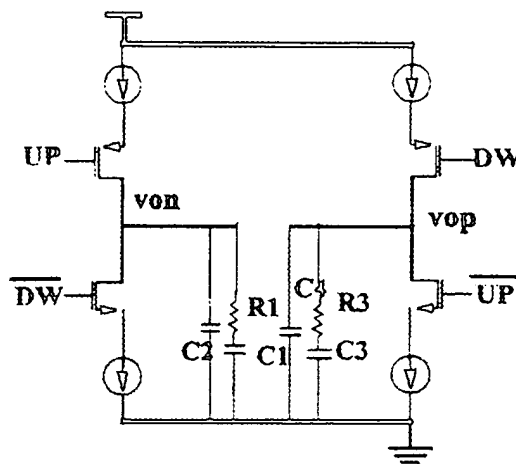


Figure 6.42 The conventional charge pump (ISSCC'95 IBM)

The charge pump cell has two charge pump circuits which are driven by **Up** and **Dw** signals. When the PLL is locked, a mismatch of current sources results in the leakage into the loop filter. This effect is periodic and produces sidebands at the output. When **Up** and **Dw** switches turn off, charge injection and clock feedthrough results in an error of control voltage, and changes the VCO frequency. The proposed charge pump shown in Fig. 6.40 suppresses any charge sharing of switching nodes by parasitic capacitance. This is why the switching does not happen at the control voltage node but stays away from it. Moreover, the cascoded stage helps in reducing switching noise by AC coupling to the bias.

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resistors R1 and R2 whenever the charge pump is turned on and off.

If the charge pump is placed under the regulated voltage ($V_c=2.2V$) for a higher PSNR from supply noise, it should be applicable in low voltage operation. A charge pump(II) is proposed in Fig. 6.41 which is more useful in low operating power supply voltage applications. The charge pump is simplified to two differential input stages, which can prevent switching coupling to the loop filter by having constant voltage sources at the input stages. The differential loop filters are replaced by a loop filter and a constant voltage for saving silicon area, which looks as if operating differentially.

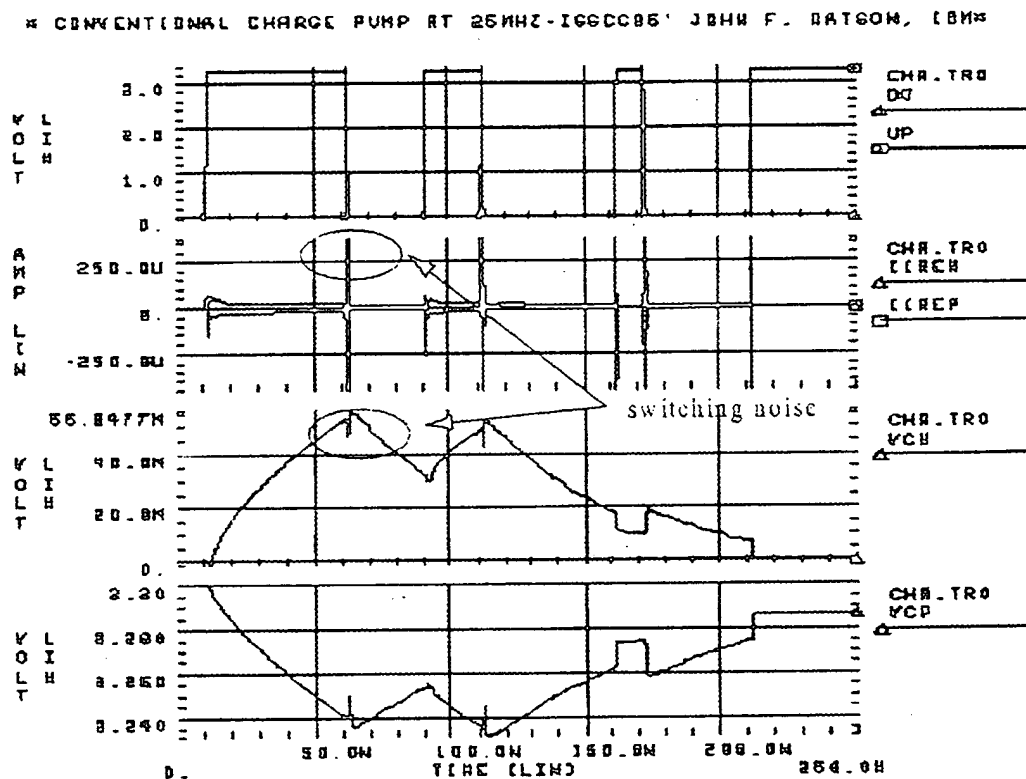


Figure 6.43 Simulated result of conventional type charge pump

On the other hand, the conventional DCP proposed by IBM experiences switching

noise problems such as charge sharing and clock feed through because UP and DW digital signals are directly applied to the LPFs (Fig. 6.42). The Fig. 6.43 and Fig. 6.44 show the simulated results of the charge pump for the conventional type and proposed type (II).

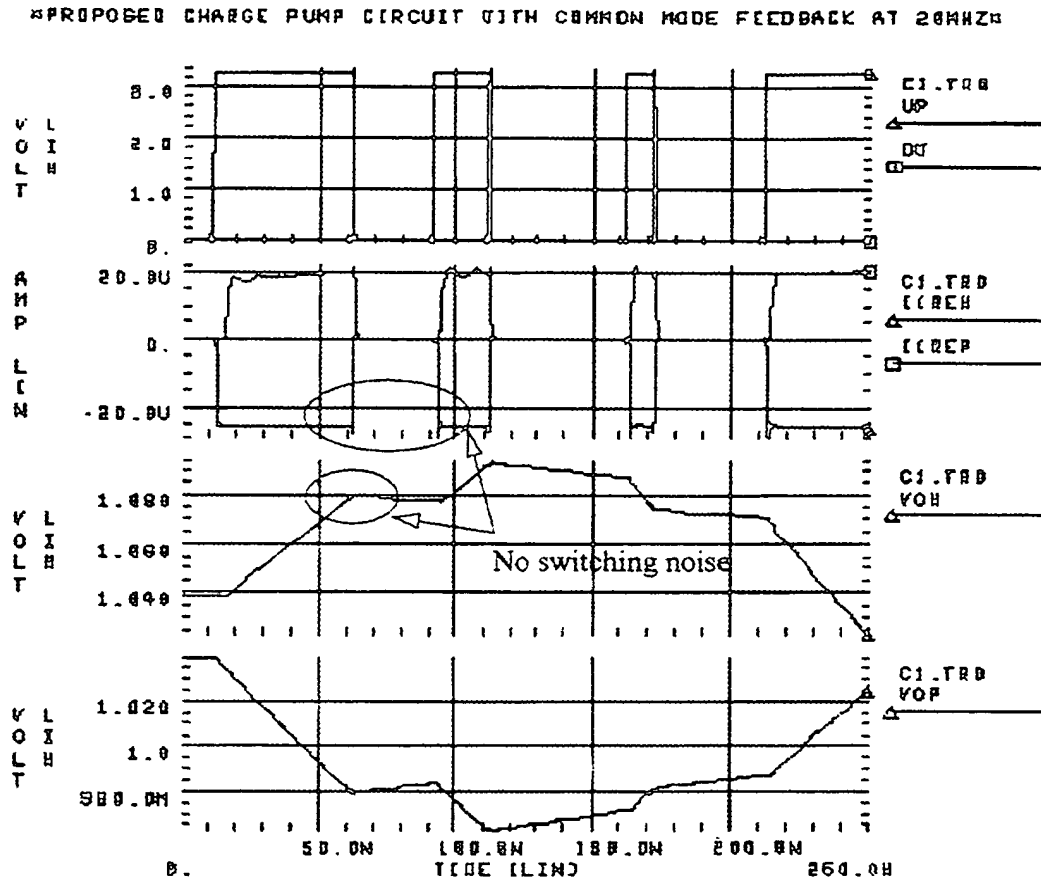


Figure 6.44 Simulated result of the proposed charge pump

Since charge pump current is a function of loop bandwidth and damping factor of the PLL, it should be designed with a stable temperature characteristics. Fig. 6.45 shows that the proposed current source using ZTC technique is compared with a positive temperature

6.3.4 Voltage to current converter

To control the frequency with a differential input voltage, a voltage to current converter is designed using a rail to rail input stage as shown Fig. 6.34.

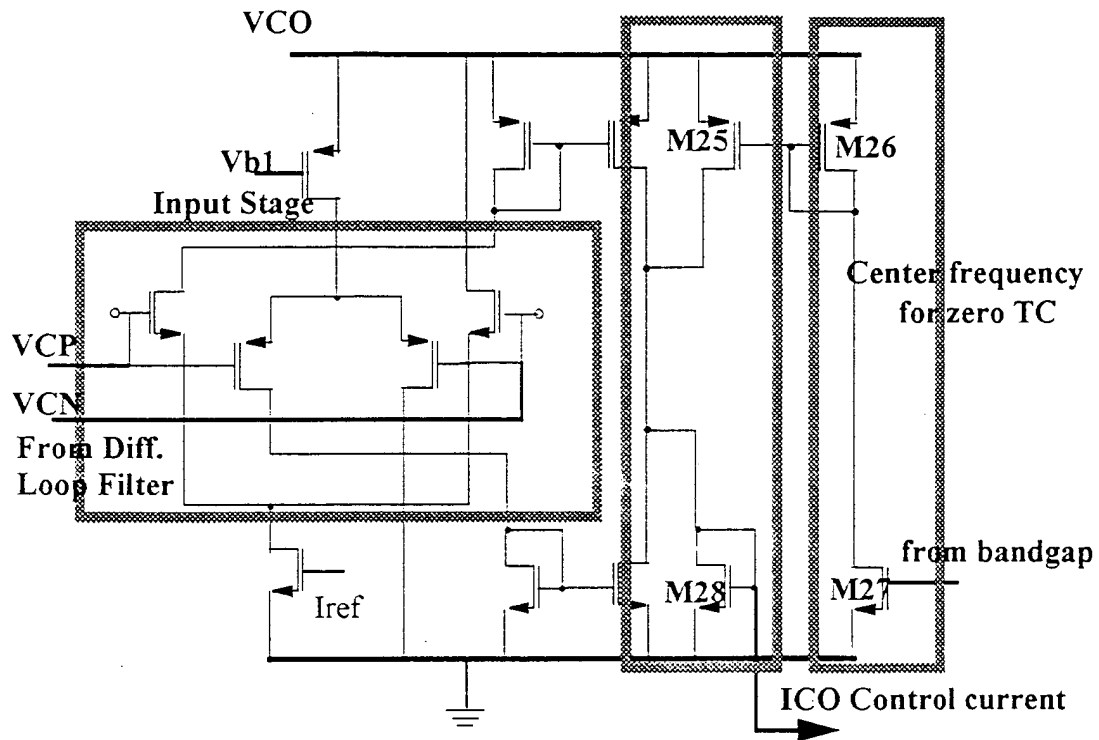


Figure 6.34 Differential voltage to single current converter

The regulated supply voltage is as low as 2.2V, so a rail to rail input stage is needed for enough common mode voltage. This transconductance provides good linearity performance with small sizes of input transistors without using resistors. Transistors MP27, MN26, and MP25 offer a constant current source for the center frequency when the voltage difference of the differential loop filter is zero. This current source generating the center frequency is close to the PLL output frequency after being locked. This is for

increasing the dynamic range of the V2I converter. The simulation result of the V2I circuit is shown as Fig. 6.35.

In the differential voltage input to current converter circuit, there is no dominant pole to degrade PLL system stability. High speed operation in the current mode circuits results from the small voltage swing of each low impedance node, operation near frequency f_T and wide band frequency response [35], [36], [37], [38].

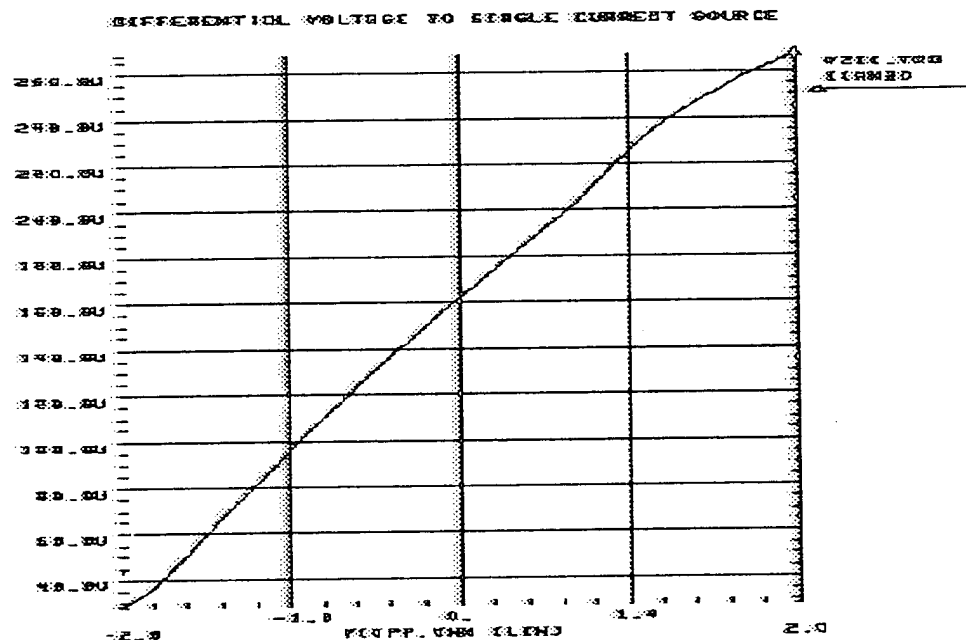


Figure 6.35 The simulated result of differential voltage to current output

6.3.5 Phase frequency detector

A type-four phase/frequency detector with D flip-flop and RS latch is simulated and implemented in the design. A typical implementation is shown as Fig. 6.36. If the state

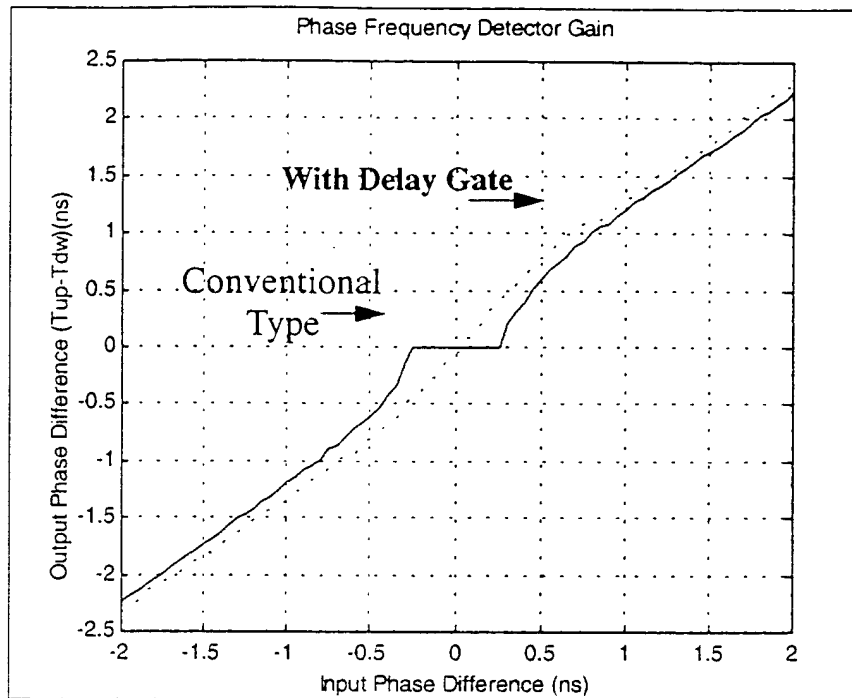


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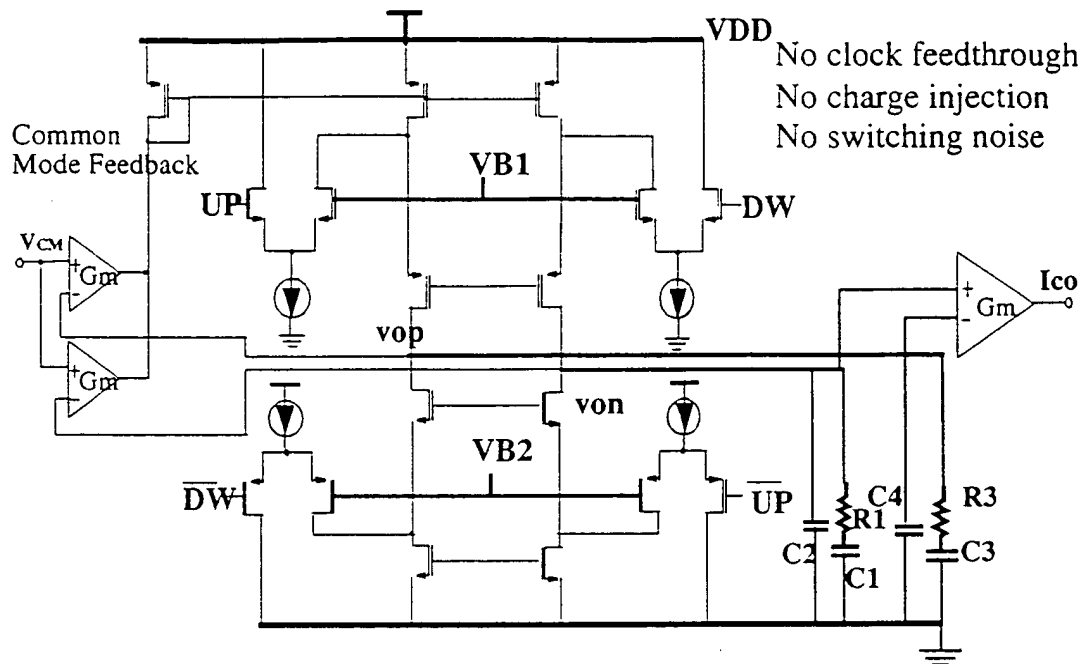


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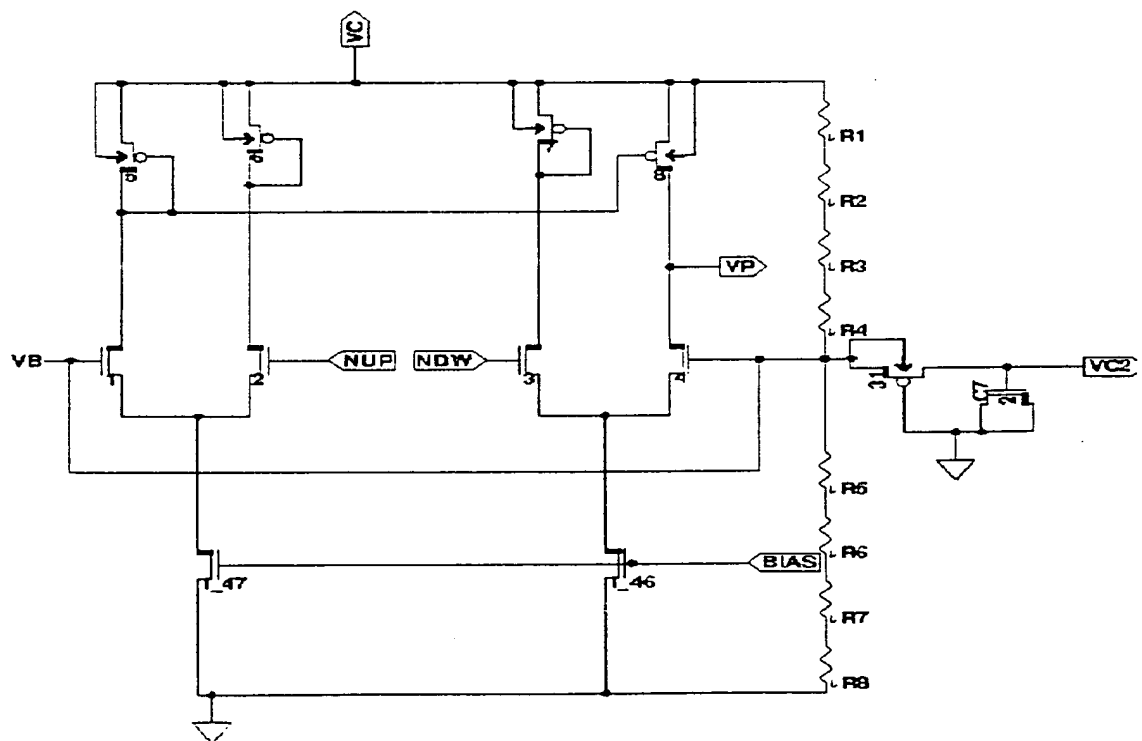


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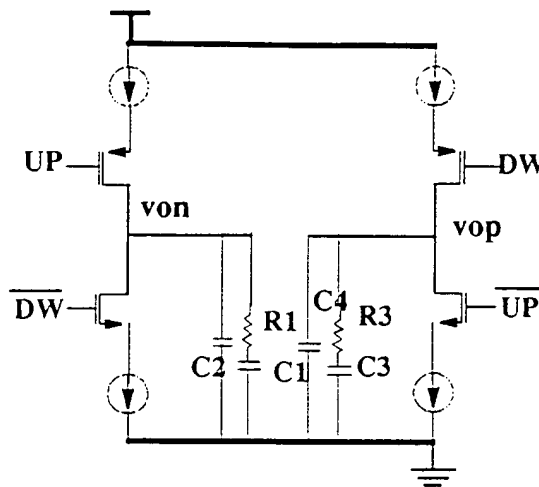


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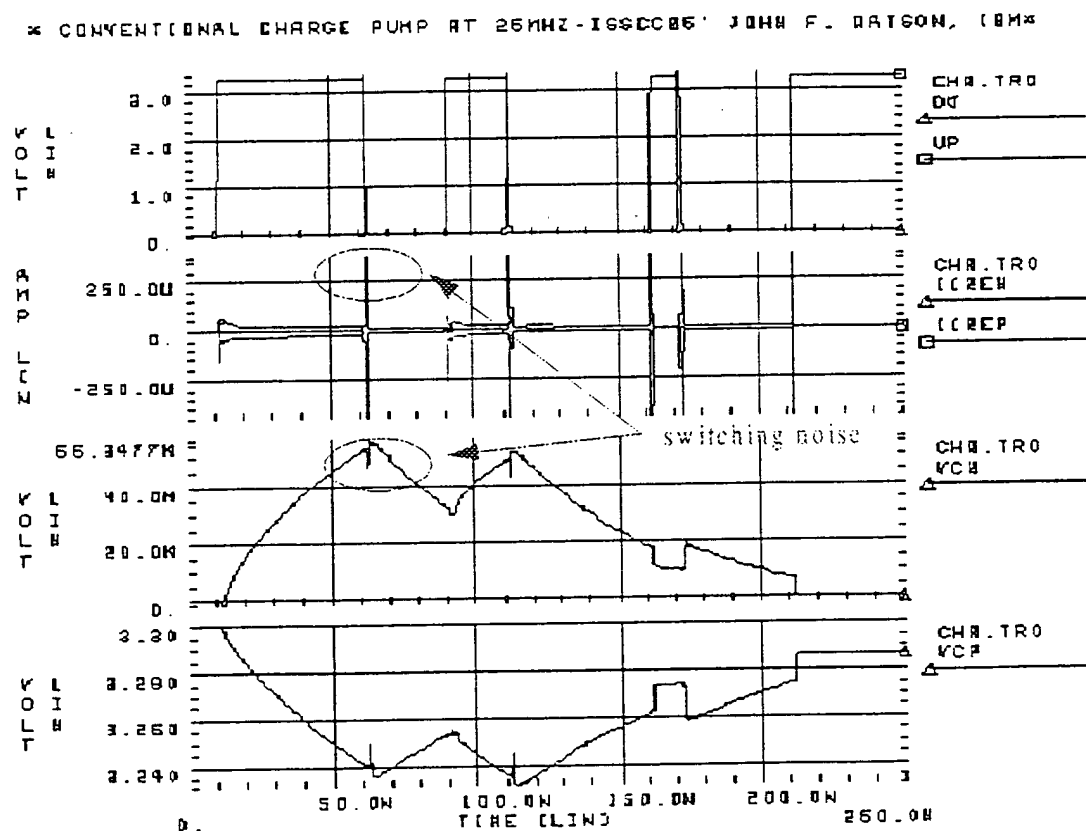


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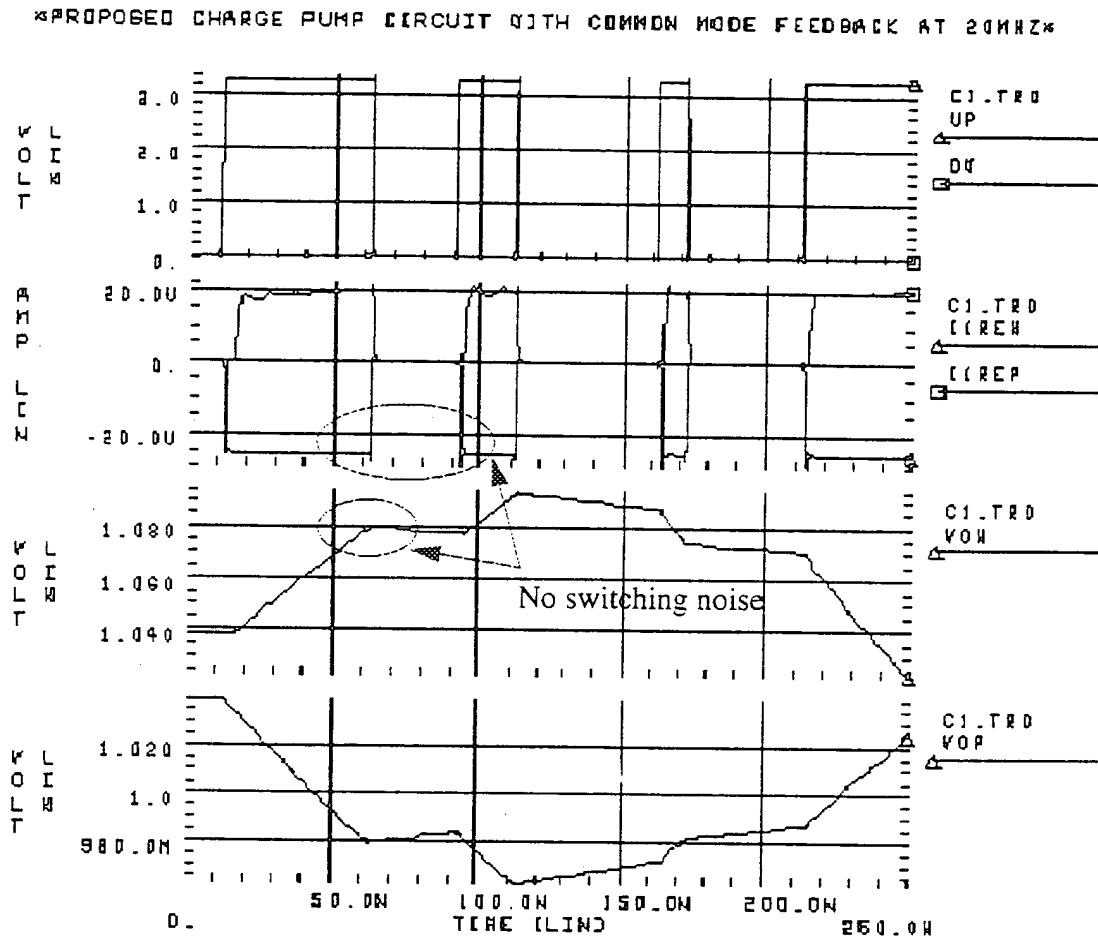


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Formal Mr. Chang-Hyeon Lee	

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Location:	Newport Beach
Department Number:	776
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Mail Stop:	601
Manager:	Mr. Pete Good

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